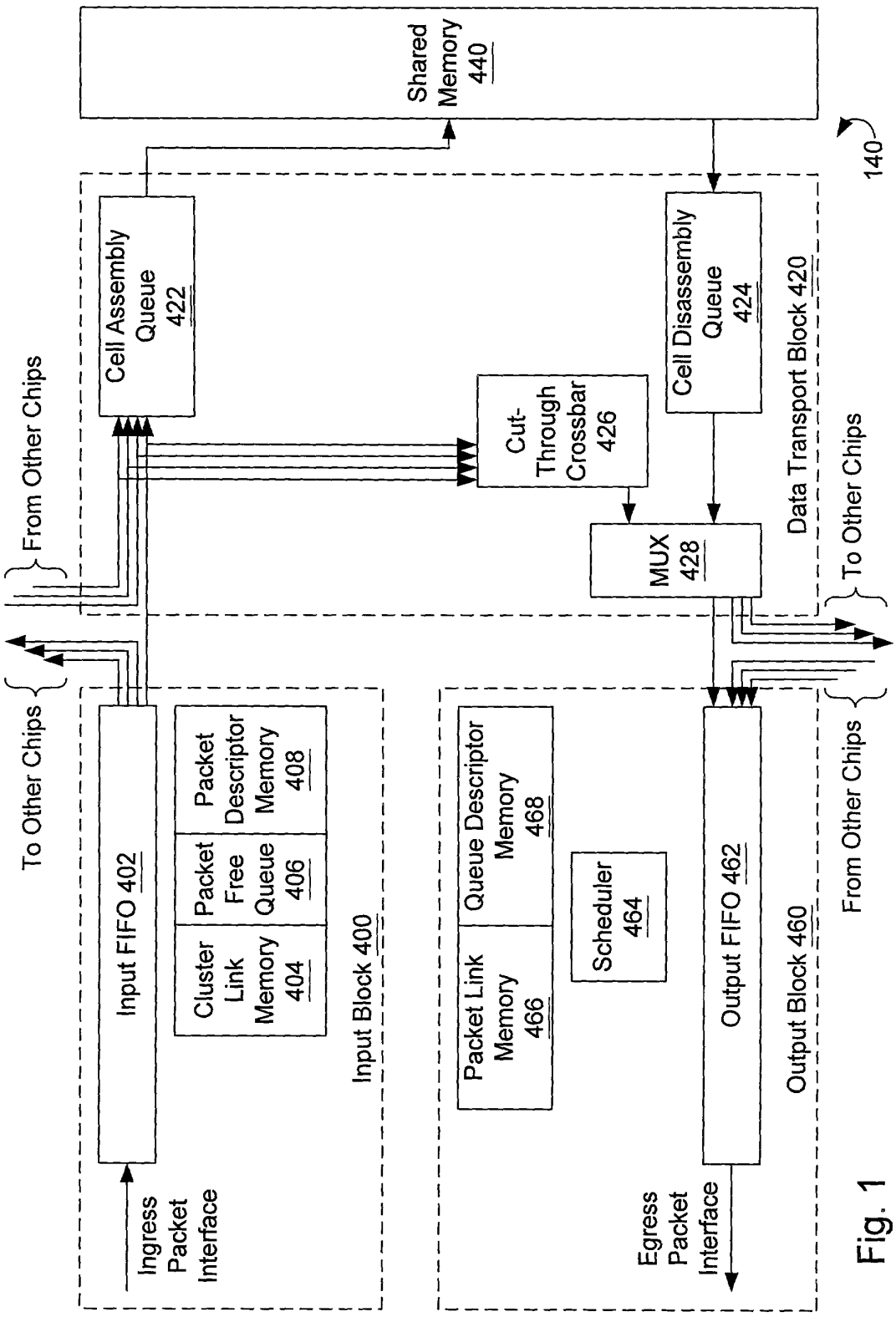
Shared Memory 440
140
Cell Assembly Queue 422
Cut-Through Crossbar 426
Cell Disassembly Queue 424
From Other Chips
MUX 428
Data Transport Block 420
To Other Chips
To Other Chips
Input FIFO 402
Packet Descriptor Memory 408
Packet Free Queue 406
Cluster Link Memory 404
Input Block 400
Queue Descriptor Memory 468
Packet Link Memory 466
Scheduler 464
Output FIFO 462
Output Block 460
From Other Chips
Ingress Packet Interface
Egress Packet Interface

Fig. 1

Field Name	Size (in bits)	Description
Queue Count 490A	5	This field is the number of output queues that contain this packet. When a packet is received, this field is initially set to the number of output queues on which the packet is inserted. This value is the number of 1 bits (i.e., asserted bits) in the port mask of the flow descriptor (after the source port has been removed from the mask). This field will be decremented as each output queue transmits the packet until the count reaches 0 when the packet (descriptor and cell memory) will be freed. This field may be stored in a separate queue count memory.
Cluster Count 490B	7	This field stores the number of clusters used by the packet. This is used by the read stored packet Manager to indicate how many clusters are to be freed when a packet is either read out or discarded.
Input Flow Number 490C	10	This field is used to track resources per flow and to update resources when the packet is freed.
Threshold Group / Virtual Channel Number 490D	5	This field is used to track resources per threshold group and to update resources when the packet is freed. The MSB (most significant bit) of this field indicates if the lower bits are group or VC (virtual channel) number: 1 = threshold group (4 bits) 0 = VC number (3 bits)
Cell List Head 490E	15	This field points to the first cell (cluster) of the packet's data. Note a linked list of cells (clusters) holds the packet data.
Cell List Tail 490F	15	This field points to the last cell (cluster) of the packet's data. Note a linked list of cells (clusters) holds the packet data.
Tail Valid 490G	1	This field indicates whether the packet has completely been written to memory as of the time that the packet descriptor is written, and thus whether the tail cell pointer is valid. This is used by the read stored packet manager in the case of an early-forwarded packet.
Error Detected 490H	1	This field indicates whether any error has been detected by the fabric before writing to memory. This bit is the ERR (error) bit of the packet. It is written at the end of a packet, when the Cell List Tail and Tail Valid signals are updated. For multiple cell packets, this bit is cleared on the first write of the packet descriptor.
To Be Dropped 490I	1	This bit indicates that the packet is to be dropped when it is scheduled. This occurs for packets when resources are depleted after it has already begun to be written to memory. In some embodiments it may be guaranteed that this packet is never early-forwarded, and thus can be dropped when it is started to be read.
Source Port 490J	5	This field contains the port from which the packet was received. This value is used when a packet is freed to adjust the resource allocation fields in the appropriate input port descriptor.
High Priority 490K	1	This field indicates if the packet is high priority. If this bit is set, the packet is not subject to thresholding. The packet is only dropped if there are no more "non-VC" (non-virtual channel) resources available.

Fig. 2

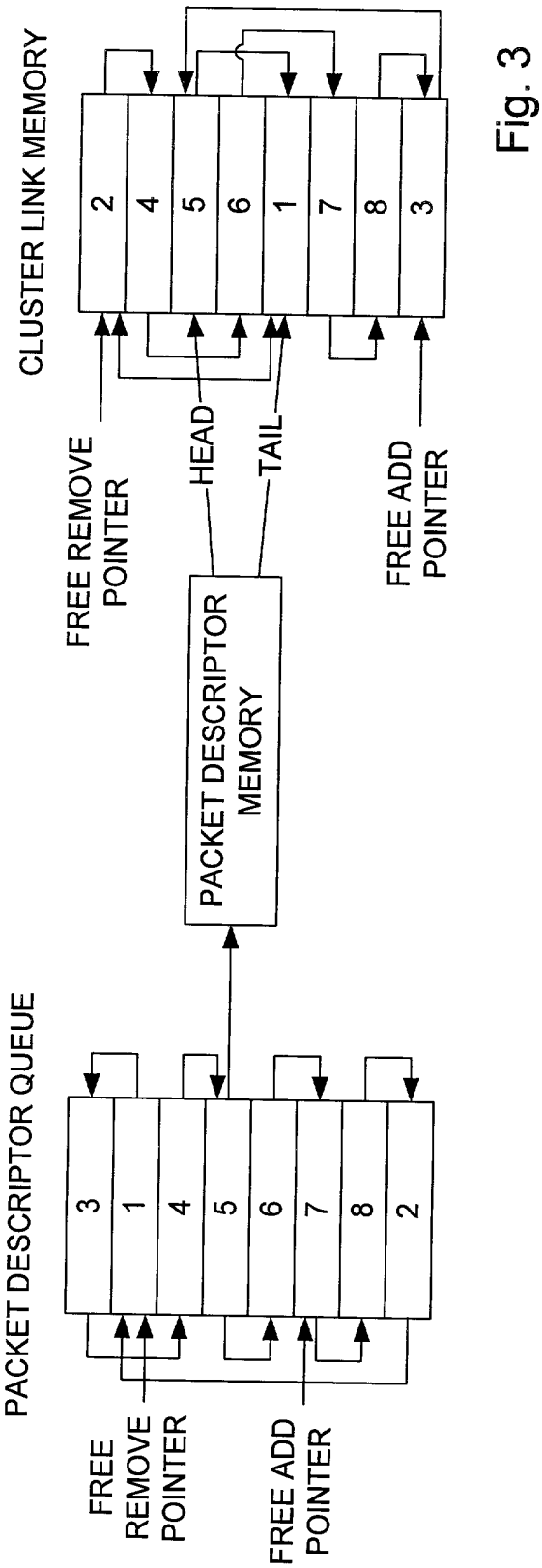
CLUSTER LINK MEMORY
2
4
5
6
1
7
8
3
FREE REMOVE POINTER
HEAD
TAIL
FREE ADD POINTER
PACKET DESCRIPTOR MEMORY
PACKET DESCRIPTOR QUEUE
3
1
4
5
6
7
8
2
FREE REMOVE POINTER
FREE ADD POINTER

Fig. 3

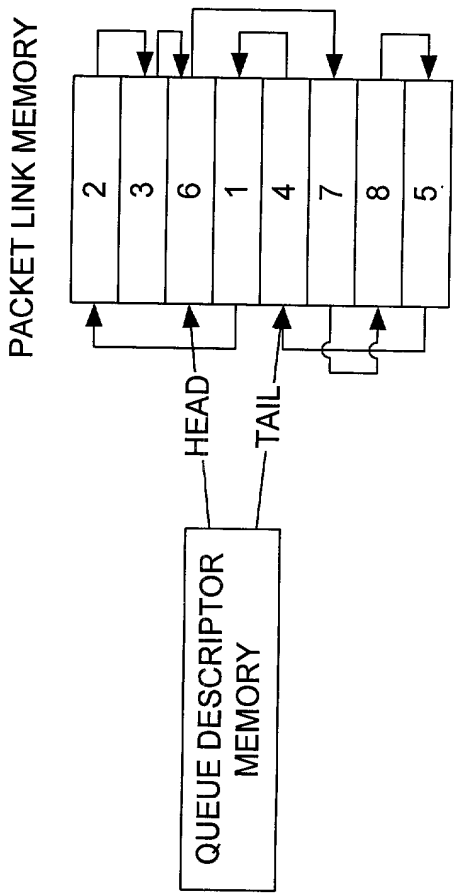
PACKET LINK MEMORY
2
3
6
1
4
7
8
5
HEAD
TAIL
QUEUE DESCRIPTOR MEMORY

Fig. 4

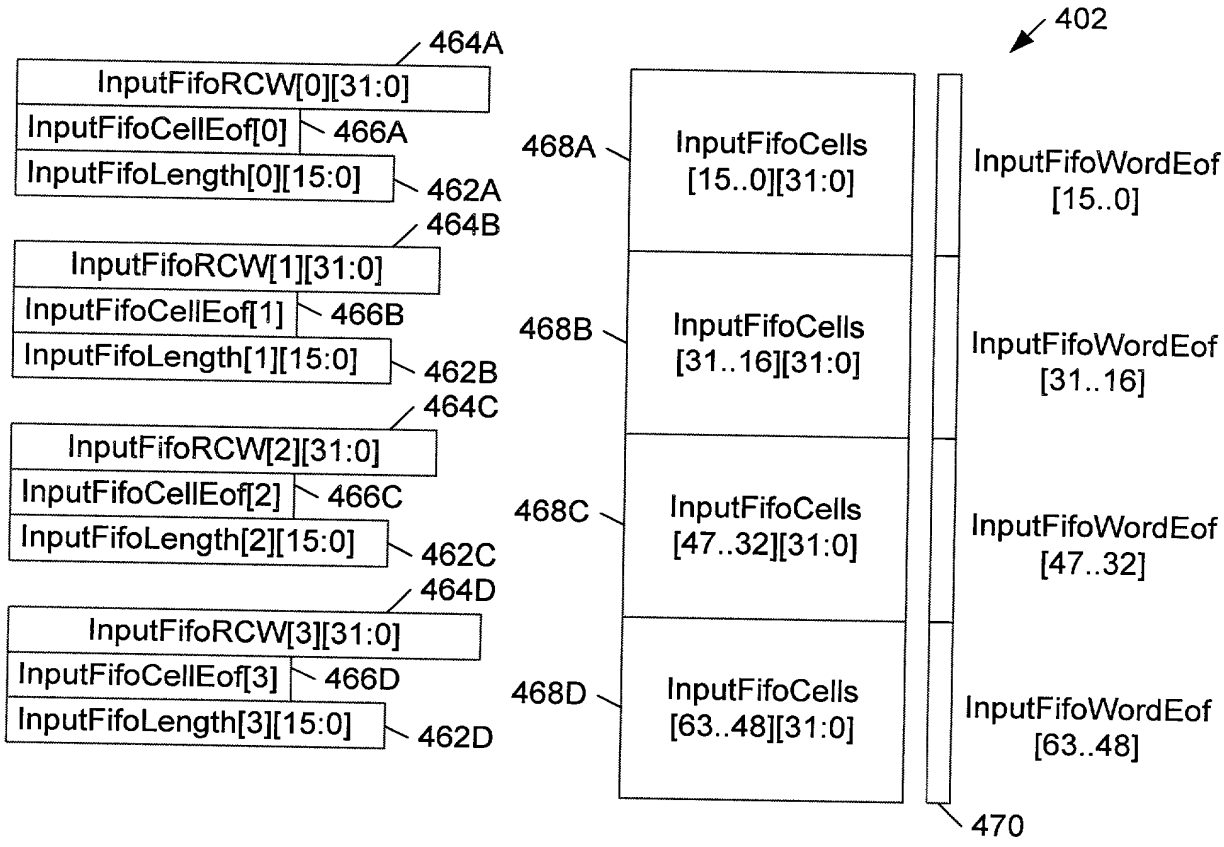

Fig. 5

	FIFO Pointer	Function
472A	***HeadCellPtr[1:0]***	Points to the current head cell
472B	***TailCellPtr[1:0]***	Points to the current tail cell
474	***SavedFirstCellPtr[1:0]***	Points to the saved first cell for the currently read packet
476	***WriteWordPtr[3:0]***	Points to the word within the tail cell that is being written to
478	***SfReadWordPtr[3:0]***	Points to the word within the head cell that is being read from for store and forward
480	***CtReadWordPtr[3:0]***	Points to the word within the head cell that is being read from for cut-through

Fig. 6

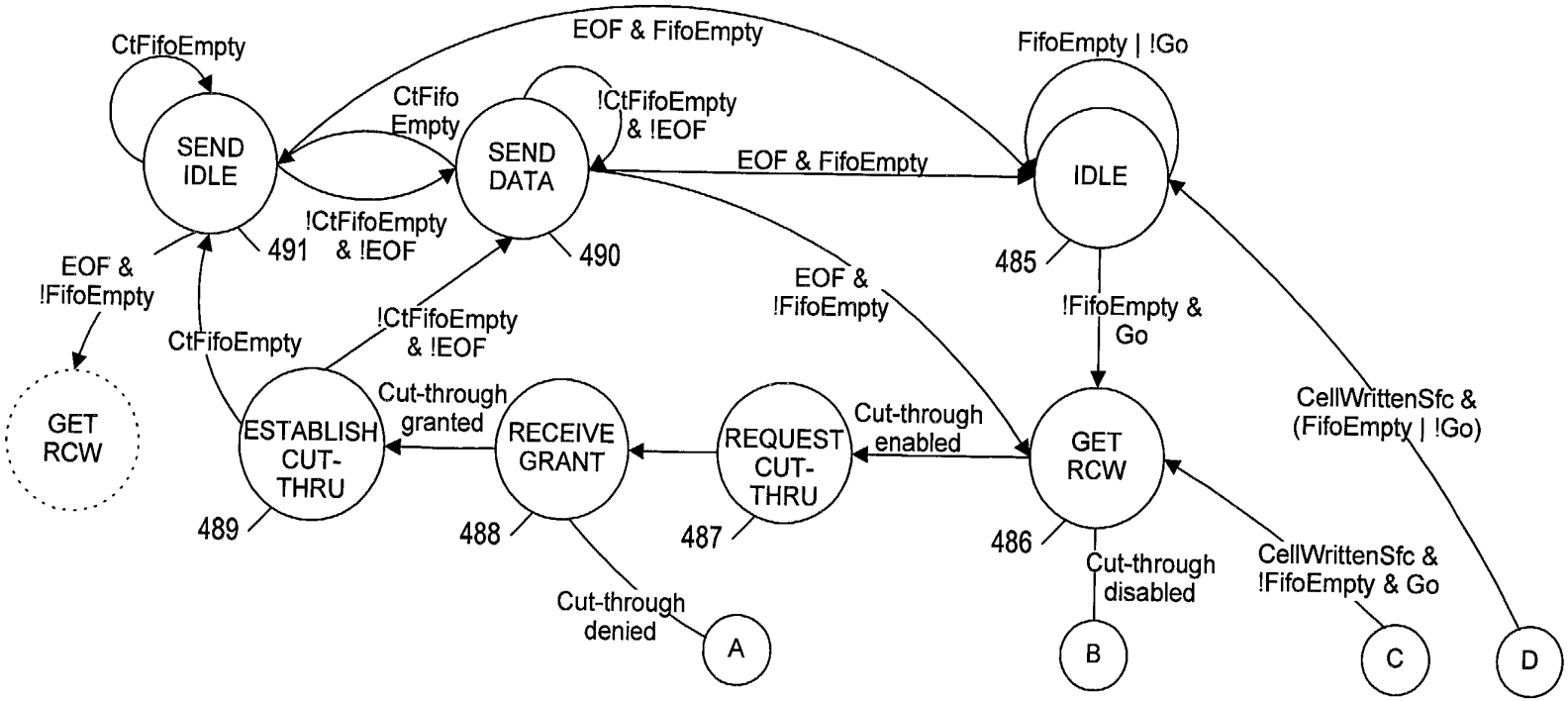
CtFifoEmpty
SEND IDLE
491
EOF & FifoEmpty
CtFifo Empty
!CtFifoEmpty & !EOF
SEND DATA
490
!CtFifoEmpty & !EOF
EOF & FifoEmpty
FifoEmpty | !Go
IDLE
485
EOF & !FifoEmpty
!FifoEmpty & Go
EOF & !FifoEmpty
GET RCW
CtFifoEmpty
!CtFifoEmpty & !EOF
ESTABLISH CUT-THRU
489
Cut-through granted
RECEIVE GRANT
488
REQUEST CUT-THRU
487
Cut-through enabled
GET RCW
486
CellWrittenSfc & (FifoEmpty | !Go)
Cut-through disabled
CellWrittenSfc & !FifoEmpty & Go
Cut-through denied
A
B
C
D

Fig. 7

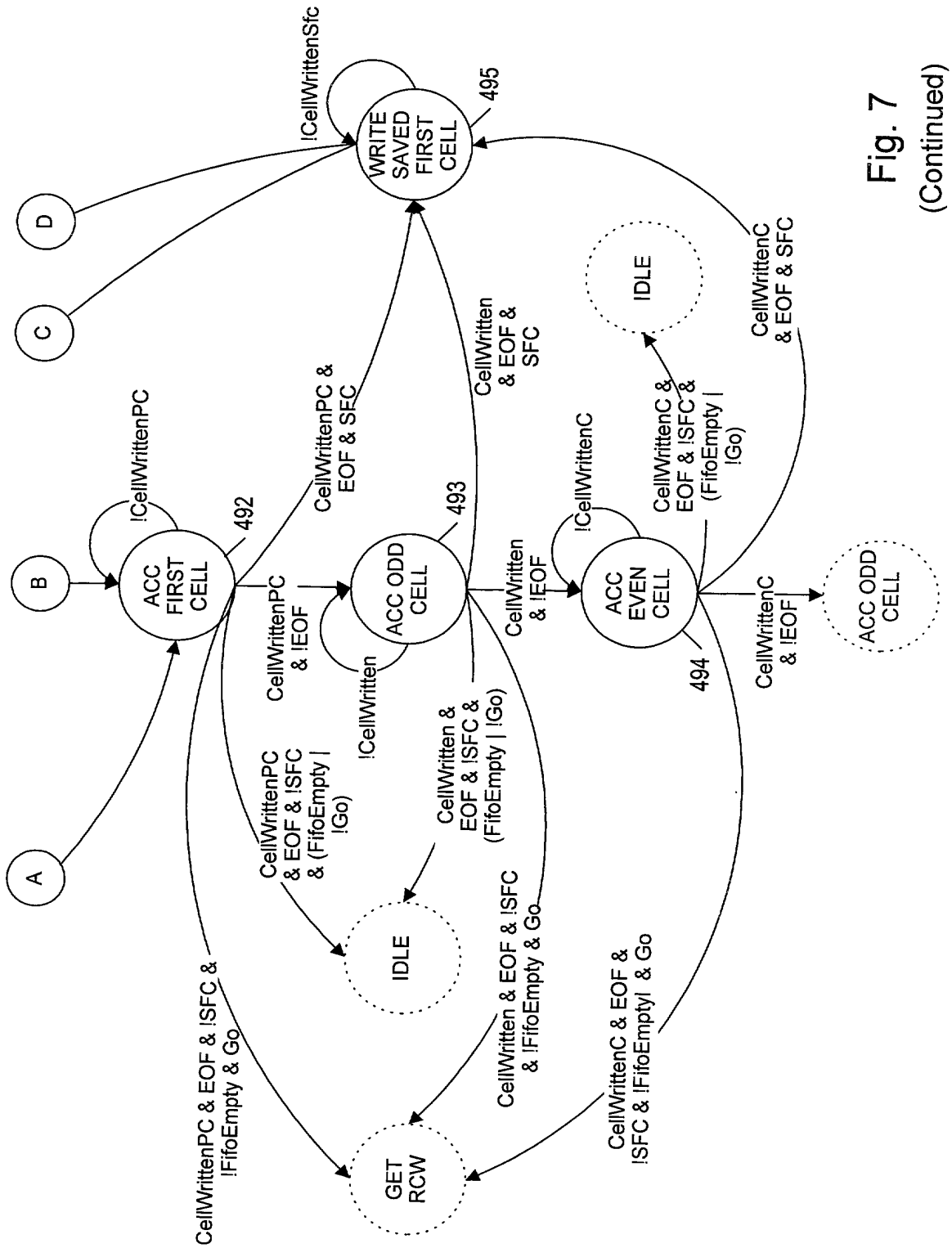

Fig. 7
(Continued)

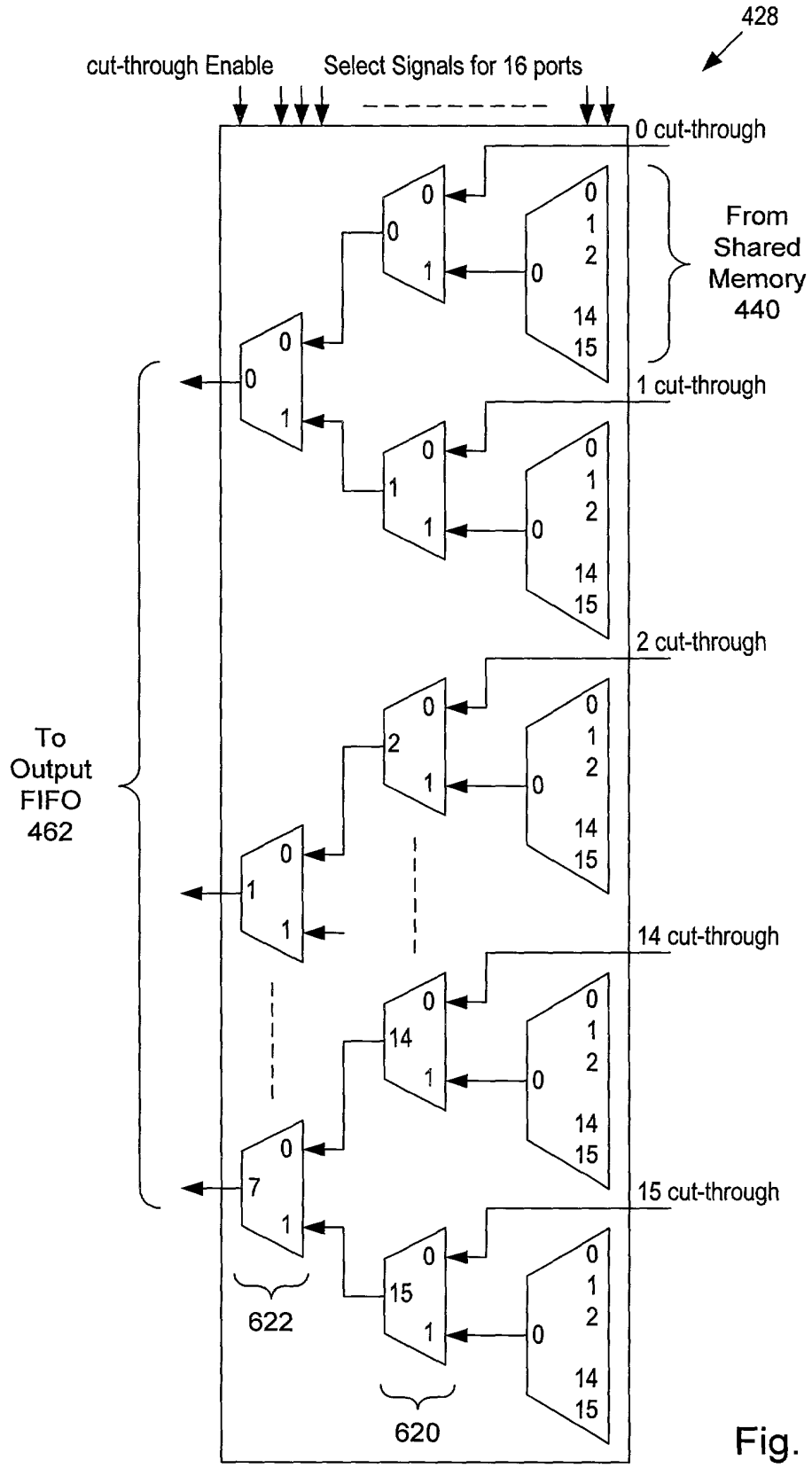
428
cut-through Enable
Select Signals for 16 ports
0 cut-through
From Shared Memory 440
1 cut-through
2 cut-through
14 cut-through
15 cut-through
To Output FIFO 462
622
620

Fig. 8

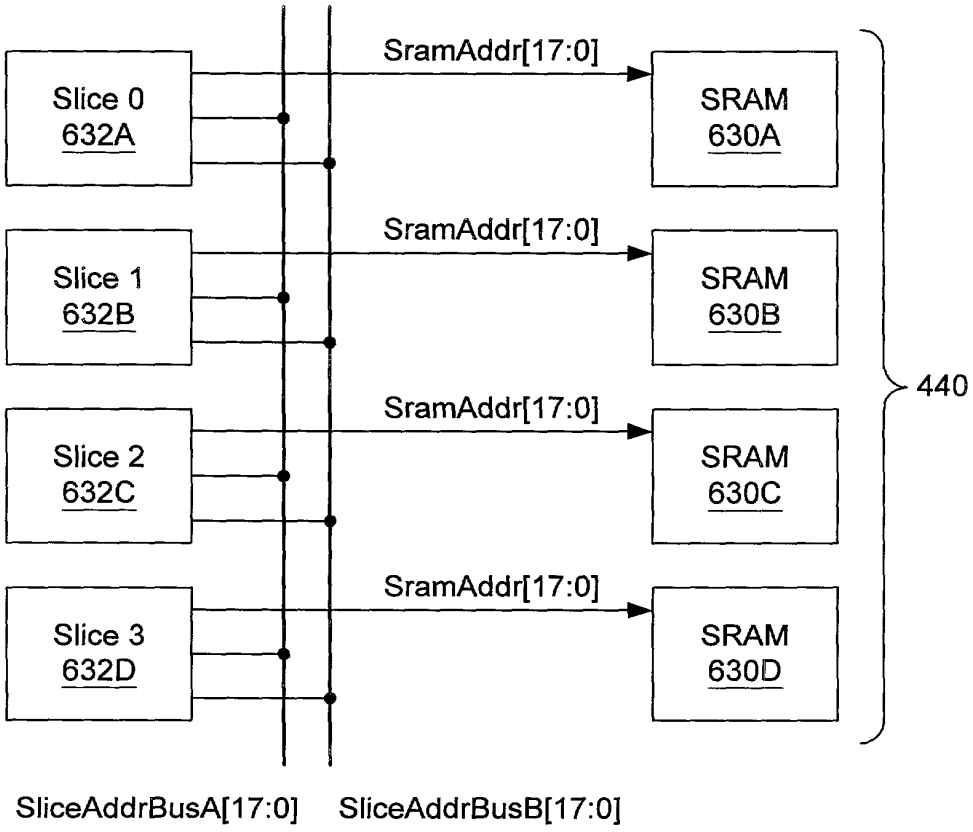
SramAddr[17:0]
Slice 0
632A
SRAM
630A
SramAddr[17:0]
Slice 1
632B
SRAM
630B
SramAddr[17:0]
Slice 2
632C
SRAM
630C
SramAddr[17:0]
Slice 3
632D
SRAM
630D
440
SliceAddrBusA[17:0]
SliceAddrBusB[17:0]

Fig. 9

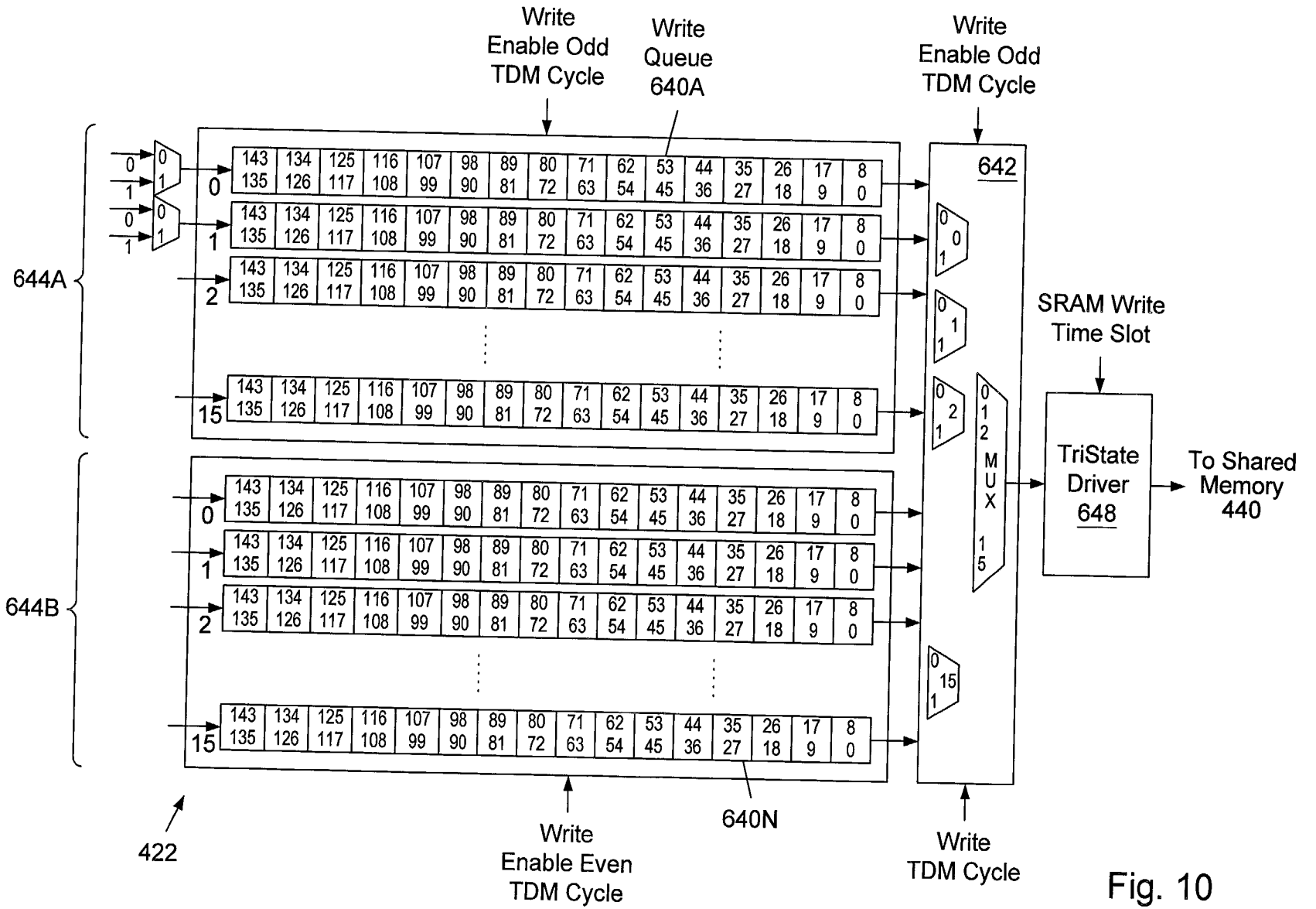
Write Enable Odd TDM Cycle
Write Queue 640A
Write Enable Odd TDM Cycle
642
644A
644B
SRAM Write Time Slot
TriState Driver 648
To Shared Memory 440
MUX
422
Write Enable Even TDM Cycle
640N
Write TDM Cycle

Fig. 10

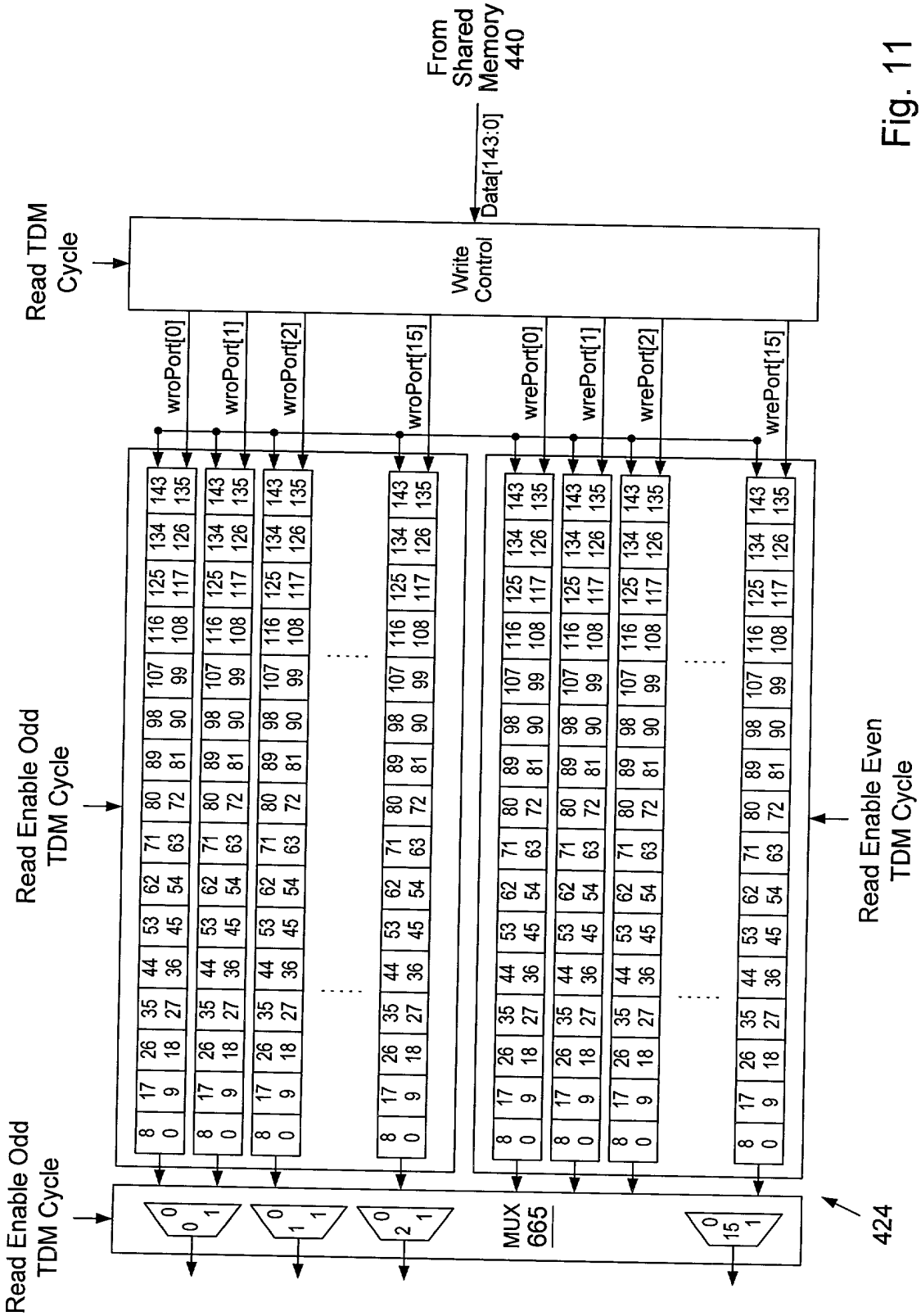
From Shared Memory 440
Data[143:0]
Write Control
Read TDM Cycle
wroPort[0]
wroPort[1]
wroPort[2]
wroPort[15]
wrePort[0]
wrePort[1]
wrePort[2]
wrePort[15]
Read Enable Odd TDM Cycle
Read Enable Even TDM Cycle
Read Enable Odd TDM Cycle
MUX 665
424

Fig. 11

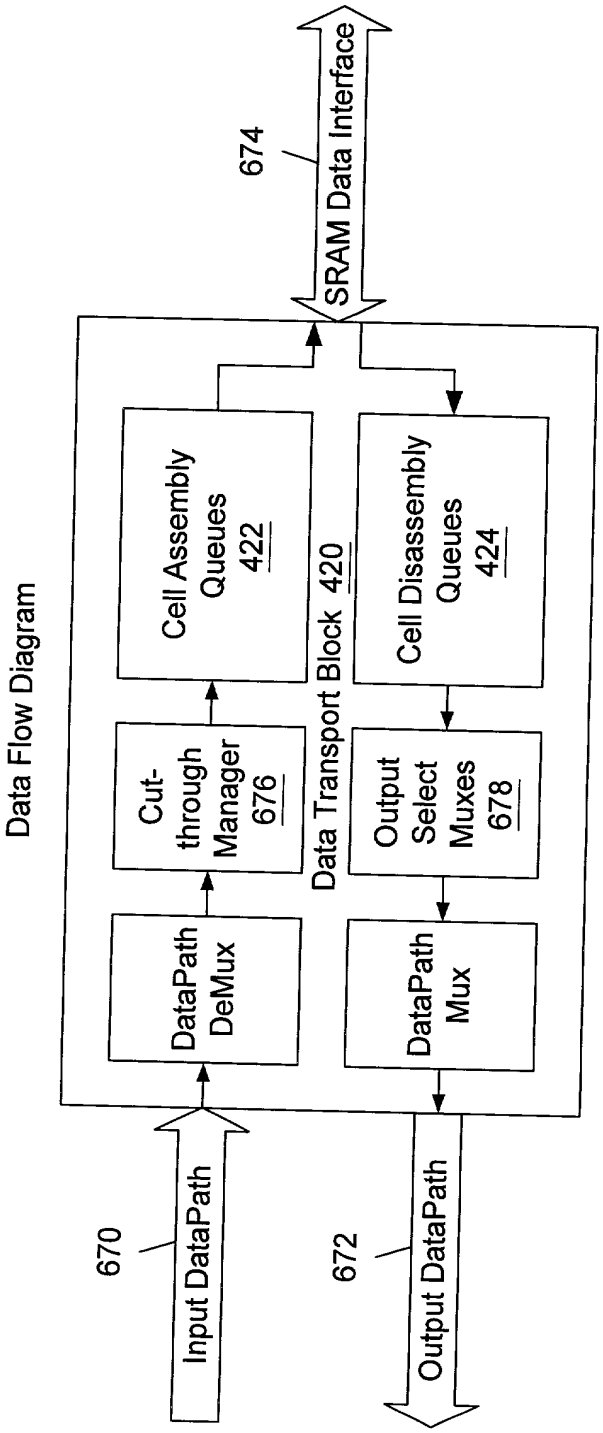
Data Flow Diagram
Data Transport Block 420
Input DataPath
670
Output DataPath
672
DataPath DeMux
Cut-through Manager 676
Cell Assembly Queues 422
DataPath Mux
Output Select Muxes 678
Cell Disassembly Queues 424
SRAM Data Interface
674

Fig. 12

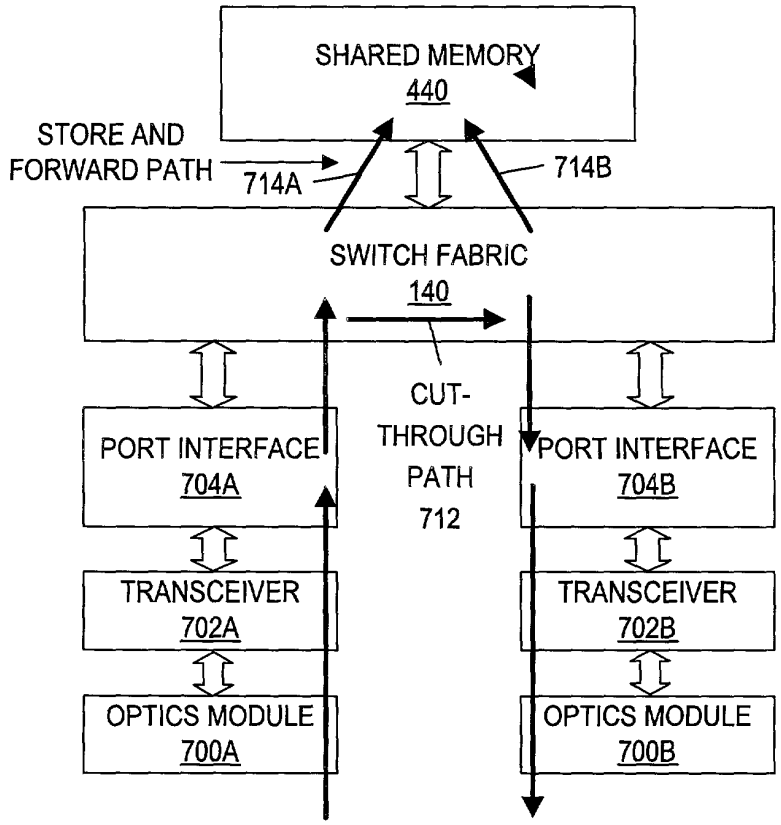
SHARED MEMORY
440
STORE AND
FORWARD PATH
714A
714B
SWITCH FABRIC
140
CUT-
THROUGH
PATH
712
PORT INTERFACE
704A
PORT INTERFACE
704B
TRANSCEIVER
702A
TRANSCEIVER
702B
OPTICS MODULE
700A
OPTICS MODULE
700B

Fig. 13

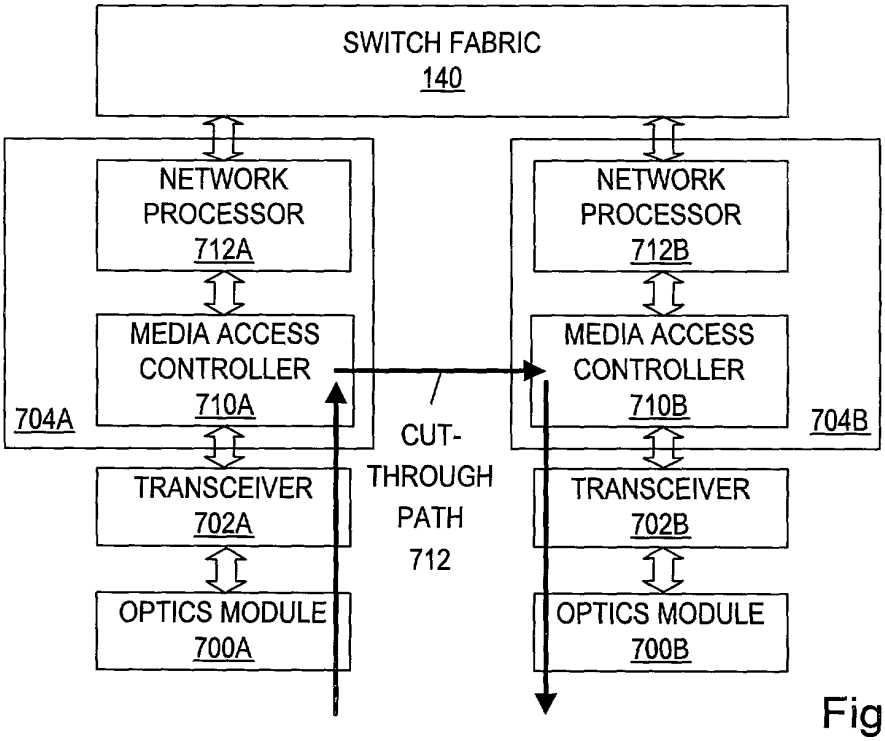
SWITCH FABRIC
140
NETWORK
PROCESSOR
712A
NETWORK
PROCESSOR
712B
MEDIA ACCESS
CONTROLLER
710A
MEDIA ACCESS
CONTROLLER
710B
704A
704B
CUT-
THROUGH
PATH
712
TRANSCEIVER
702A
TRANSCEIVER
702B
OPTICS MODULE
700A
OPTICS MODULE
700B

Fig. 14

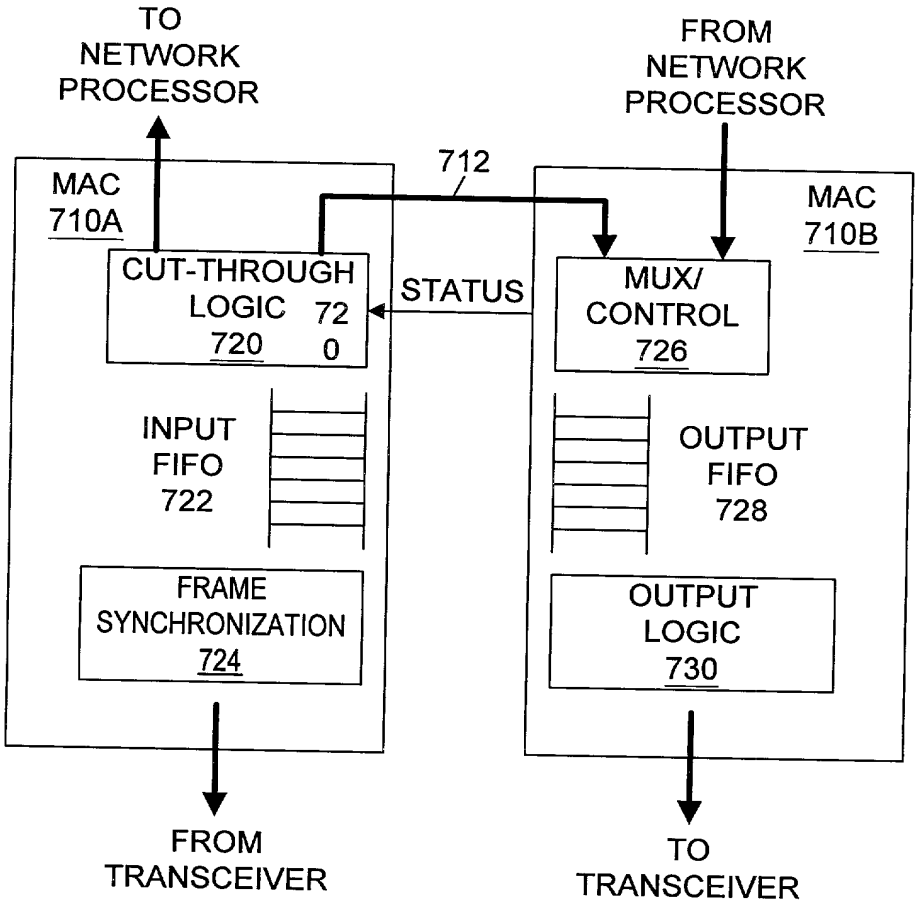

Fig. 15

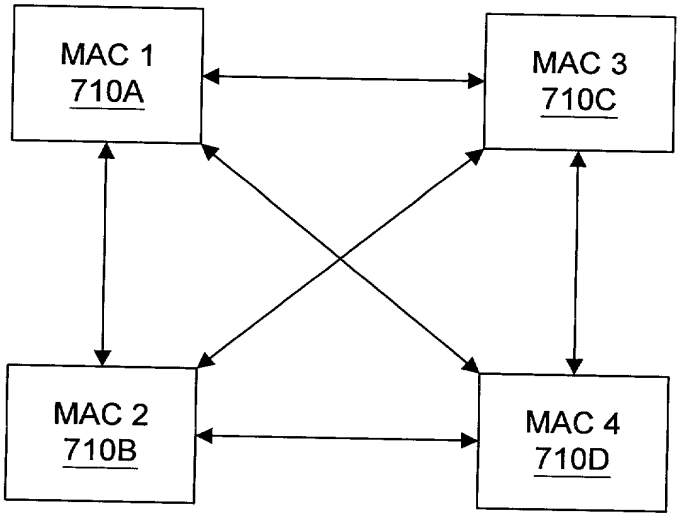

Fig. 16A

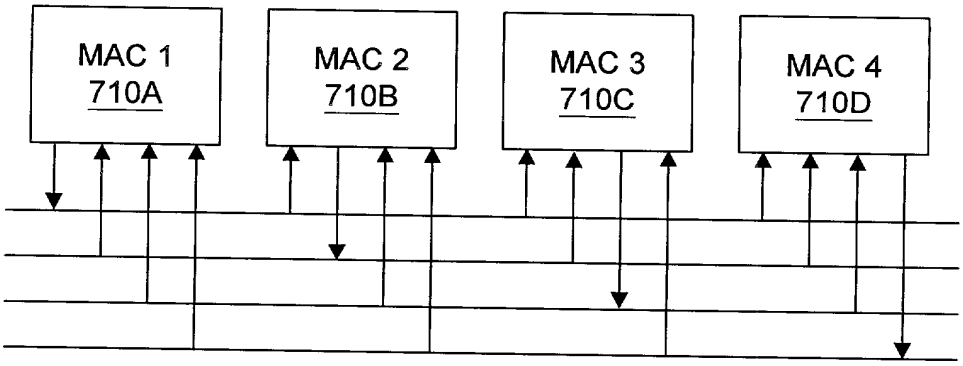

Fig. 16B

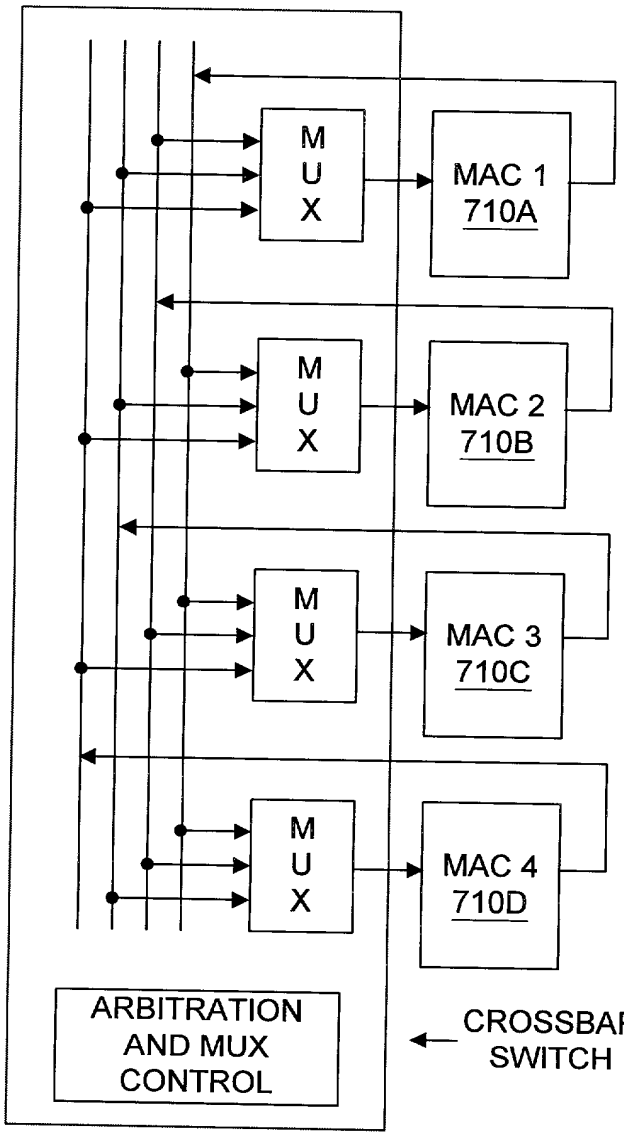

Fig. 16C

OSI MODEL

LAYER	LAYER NAME	FUNCTION
7	APPLICATION LAYER	PROGRAM-TO-PROGRAM COMMUNICATION.
6	PRESENTATION LAYER	MANAGES DATA REPRESENTATION CONVERSIONS. FOR EXAMPLE, THE PRESENTATION LAYER WOULD BE RESPONSIBLE FOR CONVERTING FROM EBCDIC TO ASCII.
5	SESSION LAYER	RESPONSIBLE FOR ESTABLISHING AND MAINTAINING COMMUNICATIONS CHANNELS. IN PRACTICE, THIS LAYER IS OFTEN COMBINED WITH THE TRANSPORT LAYER
4	TRANSPORT LAYER	RESPONSIBLE FOR END-TO-END INTEGRITY OF DATA TRANSMISSION.
3	NETWORK LAYER	ROUTES DATA FROM ONE NODE TO ANOTHER
2	DATA LINK LAYER	RESPONSIBLE FOR PHYSICAL PASSING DATA FROM ONE NODE TO ANOTHER.
1	PHYSICAL LAYER	MANAGES PUTTING DATA ONTO THE NETWORK MEDIA AND TAKING THE DATA OFF.

Fig. 17

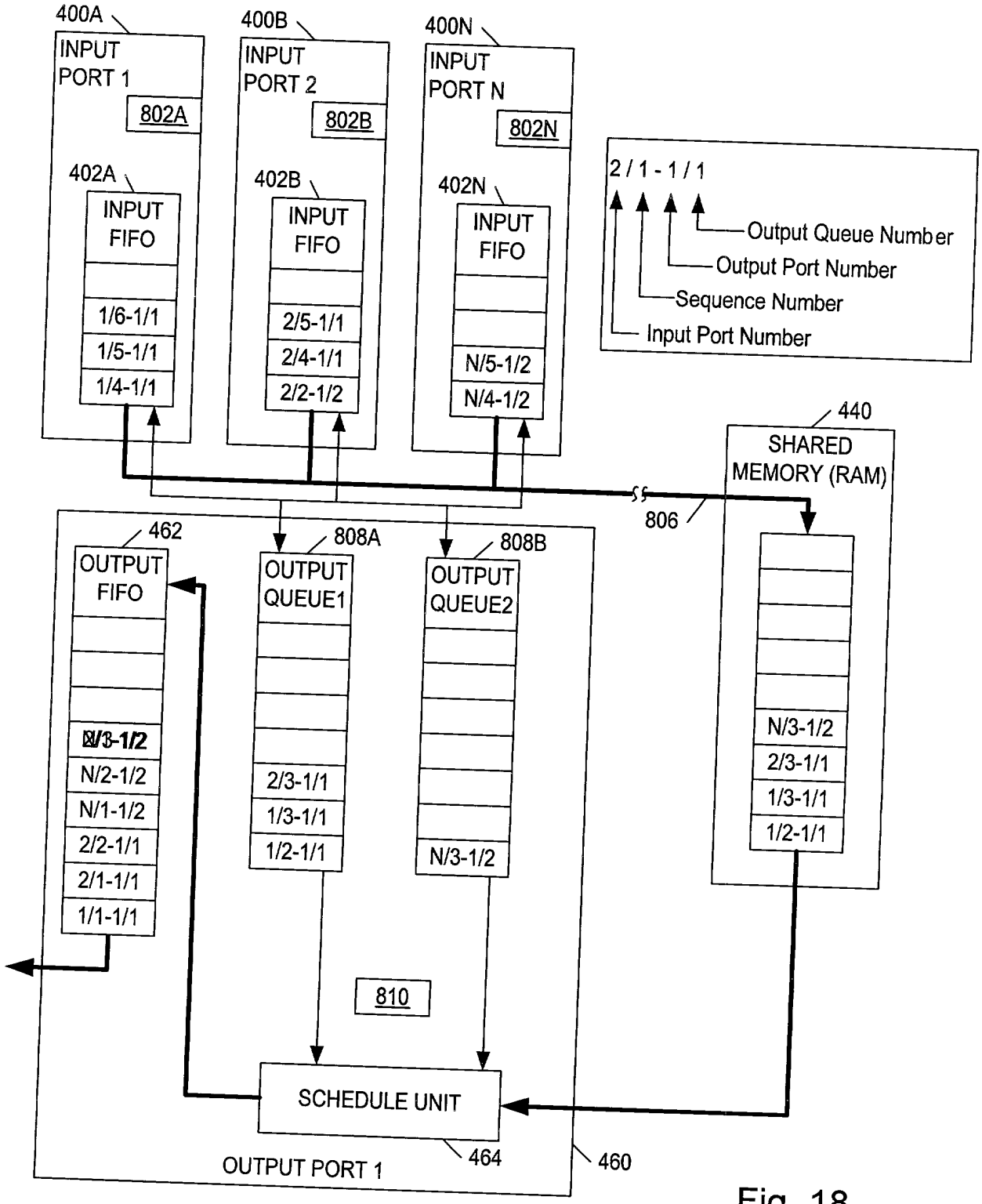
400A
INPUT PORT 1
802A
402A
INPUT FIFO
1/6-1/1
1/5-1/1
1/4-1/1
400B
INPUT PORT 2
802B
402B
INPUT FIFO
2/5-1/1
2/4-1/1
2/2-1/2
400N
INPUT PORT N
802N
402N
INPUT FIFO
N/5-1/2
N/4-1/2
2 / 1 - 1 / 1
Output Queue Number
Output Port Number
Sequence Number
Input Port Number
440
SHARED MEMORY (RAM)
806
462
OUTPUT FIFO
N/3-1/2
N/2-1/2
N/1-1/2
2/2-1/1
2/1-1/1
1/1-1/1
808A
OUTPUT QUEUE1
2/3-1/1
1/3-1/1
1/2-1/1
808B
OUTPUT QUEUE2
N/3-1/2
N/3-1/2
2/3-1/1
1/3-1/1
1/2-1/1
810
SCHEDULE UNIT
464
460
OUTPUT PORT 1

Fig. 18